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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,384	07/09/2002	Tien-Ju Tsai	7123-US-PA	4024

31561 7590 01/05/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
MEW, KEVIN D	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/064,384	TSAI ET AL.	
	Examiner	Art Unit	
	Kevin Mew	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,21 and 27* is/are rejected.

7)☒ Claim(s) *2-20 and 22-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/9/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

In particular, the abstract exceeds 150 words in length. In addition, the title of the application should be removed from the abstract page.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (USP 5,570,368) in view of Witel et al. (USP 6,721,336).

Regarding claim 1, Murakami discloses a transmission convergence sublayer circuit of an asynchronous transfer receiver (circuitry of a cell multiplexer, Fig. 1) for receiving data cells submitted from a deframer after receiving a data stream enable signal from the deframer,

wherein the data cell comprises a plurality of bytes divided into a header and a payload, the transmission convergence sublayer circuit (the circuitry comprising) comprising:

a byte-wise data pipeline (signal multiplexer, element 1, Fig. 1) for receiving and temporarily holding the data bytes in the data cell (for holding data bytes sent from the subscriber terminals, Fig. 1);

a header cyclic redundancy checker (CRC operation checker X1 of CRC operator 411-a, Figs. 8 and 10) for receiving the data bytes (for receiving data bytes from memory 2, Fig. 8) and transmitting a syndrome code (transmitting a result of the CRC operation) capable of indicating the presence a header cell (to detect the presence of position of the HEC portion of an ATM cell, col. 5, lines 63-65, col. 7, lines 51-60, 65-67, col. 8, lines 1-6, 24-39);

an idle cell identifier (selector 433, Fig. 8) for deciding whether the data cell received by the byte-wise data pipeline is a non-idle data cell or not (for deciding whether the received cell is idle cell or real cell received from the signal multiplexer via memory 2, Fig. 8);

a cell delineation state machine (delineation state controller 412, Fig. 8) for determining a transmission state of the data cell (determining the state, col. 6, lines 1-20) according to a content (according to the CRC operation result) and frequency of the syndrome code (and the number of times of continuous detection of the HEC portion via the CRC operation result, col. 6, lines 13-30, col. 7, lines 66-67, col. 8, lines 1-6) and transmitting state signals reflecting a current state (reflecting whether the state is Hunt, PreSync or Sync, col. 6, lines 1-30), wherein possible states at least include a search state (Hunt state, Fig. 5) and a complete synchronization state (Sync State, Fig. 5);

a byte pointer (write address table) for issuing a pointer signal, wherein the pointer signal indicates a sequence number of the byte belonging to the data cell (line identification number of the cell signal, Fig. 3) received by the byte-wise data pipeline (received from the signal multiplexer, col. 5, lines 1-12 and Fig. 3) and serves as an address pointer (serve as an address pointer) for sending double word data converted from newly received bytes into a buffer (for the cell signal to written into a position of memory 2 indicated by the write address, col. 5, lines 1-12);

a write-in buffer controller (write controller 311 of memory controller 3, Fig. 3) for writing the data into the buffer (for writing data to memory 2, Fig. 3) according to the indication provided by the byte pointer when permission to do so is granted by the idle cell identifier and the cell delineation state machine (according to the position indicated by the write address based on a signal indicating the position of the HEC portion supplied by the delineation state controller 412, col. 5, lines 1-12, col. 10, lines 55-59).

Murakami does not explicitly show a descrambler for descrambling a plurality of bytes residing temporarily in the byte-wise data pipeline and sending resulting descrambled data to the buffer.

However, Witel discloses a descrambler to descramble ATM cell payload and transmits the descrambled data to a FIFO memory (col. 10, lines 11-26 and Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system and method of cell processing of Murakami with the teaching of Witel in using a descrambler to descramble ATM cell payload such that a descrambler can be incorporated in the cell multiplexer of Murakami for descrambling a plurality

of bytes residing temporarily in the byte-wise data pipeline (signal multiplexer) and sending resulting descrambled data to the buffer (memory).

The motivation to do is to descramble the information field carrying the ATM cell payload data.

3. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (USP 5,570,368) in view of Nishida et al. (USP 5,966,447).

Regarding claim 21, Murakami discloses a method of operating the transmission convergence sublayer of an asynchronous transfer receiver capable of receiving a data cell and a data stream enable signal from a deframer, wherein the data cell can be divided into header bytes and payload bytes, the operating method comprising the steps of:

a byte-wise data pipeline receiving a plurality of data bytes, wherein the byte-wise data pipeline not only receives but also temporarily holds a specific number of bytes in sequence;

a header cyclic redundancy checker (CRC operation checker X1 of CRC operator 411-a, Figs. 8 and 10) for receiving a plurality of data bytes (for receiving data bytes from memory 2, Fig. 8) and determining if a header is received (to detect the presence of position of the HEC portion of an ATM cell, col. 5, lines 63-65, col. 7, lines 51-60, 65-67, col. 8, lines 1-6, 24-39), wherein a syndrome code representing the presence or absence of a header is issued (issuing a result of the CRC operation);

a cell delineation state machine (delineation state controller 412, Fig. 8) determining if a state transition from a search state to a full synchronization state is carried out (determining if a state transitions from a Hunt state to a Sync state, col. 6, lines 1-20) according to the syndrome

code (according to whether the HEC portion is detected via the CRC operation result) and the number of times of continuous detection of the HEC portion, col. 6, lines 13-30, col. 7, lines 66-67, col. 8, lines 1-6); and

a byte pointer (write address table) outputting a pointer signal (line identification number, col. 5, lines 1-12) according to the state indicated by the cell delineation state machine (according to the delineation sate, element 42-a, Fig. 8) for pointing out the sequence number of the newly received bytes belonging to the data cell (line identification number of the cell signal, Fig. 3) as well as the storage address of the data (the write address indicating the position of memory in which to write the cell signal, col. 5, lines 1-12 and Fig. 3).

Murakami does not explicitly show a descrambler acquiring data bytes capable of descrambling out a double word into the byte-wise data pipeline in parallel after stepping into the full synchronization state in preparation for descrambling.

However, Nishida discloses a descrambler for descrambling data and outputs descrambled data into parallel bits while the descrambler is in synchronization state (col. 18, lines 49-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system and method of cell processing of Murakami with the teaching of Nishida in using a descrambler for descrambling data and outputs descrambled data into parallel bits while the descrambler is in synchronization state such that Murakami will incorporate a descrambler acquiring data bytes capable of descrambling out a double word into the byte-wise data pipeline in parallel after stepping into the full synchronization state in preparation for descrambling.

The motivation to do so is to eliminate the troubles in converting the descrambled data in binary data into byte format by serial to parallel conversion.

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (USP 5,570,368) in view of Nishida et al. (USP 5,966,447), and in further view of Diaz et al. (USP 5,537,400).

Regarding claim 27, Murakami and Nishida disclose all the aspects of claim 21 above, except fails to disclose the method of claim 21, wherein the method further includes a buffer address setting step for retrieving a specified number of the highest effective bits to serve as a buffer input address.

However, Diaz discloses that address for buffer is derived from a buffer pointer that is a 10-bit representation of one buffer in a common buffer area (col. 15, lines 51-64 and Fig. 16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system and method of cell processing of Murakami and Nishida with the teaching of Diaz in setting up a buffer address based on a 10-bit representation such that the system and method of cell processing in Murakami will include a buffer address setting step for retrieving a specified number of the highest effective bits to serve as a buffer input address.

The motivation to do so is to provide the ability to generate buffer addresses from buffer pointers.

Allowable Subject Matter

5. Claims 2-20, 22-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, the circuit of claim 1, wherein the transmission convergence circuit further includes a cell counter for responding to conditions requiring the cell delineation state machine to change from a search state into a complete synchronization state and vice versa according to the pointer signal submitted by the byte pointer, and the cell counter acts by first counting number of received data cells after the state transition and deciding if going into the complete synchronization state or returning to the search state is necessary.

Regarding claim 3, the circuit of claim 1, wherein the header cyclic redundancy checker sequentially inspects all the received bytes, and the checker further includes a compensation circuit having a compensation source whose data is derived from registered payload data within the byte-wise data pipeline.

Regarding claim 5, Murakami discloses all the aspects of claim 1 above, except fails to explicitly show the circuit of claim 1, wherein the header cyclic redundancy checker generates the syndrome code by dividing the newest five bytes of data received in parallel from the byte-wise data pipeline by a polynomial $(X^8 + X^6 + X^2+1)$.

Regarding claim 6, the circuit of claim 1, wherein the cell delineation state machine also outputs a secondary state signal that represents a next state, the byte pointer within the cell delineation state machine further includes a decoder and the decoder outputs a fourth byte signal indicating acquisition of a fourth byte into the byte-wise data pipeline according to the pointer signal from the byte pointer, the byte pointer uses the fourth byte signal and the secondary state signal to equalize the pointer signal corresponding to the sixth byte in the data cell and the pointer signal corresponding to the fifth byte in the data cell.

Regarding claim 7, the circuit of claim 1, wherein the byte-wise data pipeline can be divided into serially connected first, second and third register sections, wherein the first section is temporarily disabled on receiving a header from the byte-wise data pipeline for preventing the byte-wise data pipeline from taking in the header cyclic redundancy code, the second section is temporarily disabled for a period of time after the header cyclic redundancy code is blocked and intake of payload data by the byte-wise data pipeline is continued so that transfer of header cell data into the third section and hence nullification of the payload data is prevented.

Regarding claim 8, the circuit of claim 1, wherein the descrambler retrieves parallel byte data from the byte-wise data pipeline for descrambling doubleword data, and while descrambling header cell data, machine-generated values are used as descrambling parameters, and while descrambling payload cell data, previously received but still existing data in the byte-wise data pipeline are used as the descrambling parameters.

Regarding claim 9, the circuit of claim 1, wherein the transmission convergence sublayer further includes a header bit error corrector such that if a single bit error occurs in the header data, a correction code corresponding to the syndrome code of the error header is looked up from a header bit error correction table and sent to the descrambler so that the descrambler can descramble out a correct header.

Regarding claim 16, the circuit of claim 1, wherein the header cyclic redundancy checker further comprises:

a remainder compensation unit for receiving the bytes from the byte-wise data pipeline and conducting a XOR operation on the data bytes to produce remainder compensation data;

a first modulo 2 adder for conducting a modulo 2 arithmetic between the data bytes inside the data cell and the remainder compensation data to generate a first add data;

a second modulo 2 adder for conducting a modulo 2 arithmetic between the first add data and a quotient feedback data to generate a second add data;

a D-type flip-flop having an input terminal, an output terminal, an enable terminal and a clocking terminal, wherein the clocking terminal receives the synchronizing pulse, the enable signal receives the data stream enable signal so that the D-type flip-flop is enabled, the input terminal receives the second add data and the output terminal outputs a flip-flop data;

a quotient feedback unit for conducting a XOR operation of the flip-flop data from the D-type flip-flop to generate the quotient feedback data; and

a plurality of inverters for inverting some of the bits among the flip-flop data submitted from the D-type flip-flop such that the inverted bits and the non-inverted bits of the flip-flop data join together to form the syndrome code.

Regarding claim 17, the circuit of claim 1, wherein the byte-wise data pipeline further comprising:

a first OR gate having an input terminal, an inversion input terminal and an output terminal, wherein the input terminal receives one of the state signals, the inversion input terminal receives one of the pointer signals, the output terminal outputs a first ORed signal;

a first AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the first ORed signal, the second input terminal receives the data stream enable signal and the output terminal outputs a first ANDed signal;

a first D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the data bytes of the data cell, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the first D-type flip-flop is enabled, and the byte output terminal outputs a first delay byte data;

a second D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the first delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the second D-type flip-flop is enabled, and the byte output terminal outputs a second delay byte data;

a third D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the second delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the third D-type flip-flop is enabled, and the byte output terminal outputs a third delay byte data;

a fourth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the third delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the fourth D-type flip-flop is enabled, and the byte output terminal outputs a fourth delay byte data;

a second OR gate having an input terminal, an inversion input terminal and an output terminal, wherein the input terminal receives one of the state signals, the inversion input terminal receives one of the pointer signals and the output terminal outputs a second ORed signal;

a second AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the second ORed signal, the second input terminal receives the data stream enable signal and the output terminal outputs a second ANDed signal;

a fifth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the fourth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the second ANDed signal so that the fifth D-type flip-flop is enabled, and the byte output

terminal outputs a fifth delay byte data; a third AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives one of the pointer signals, the second input terminal receives the data stream enable signal and the output terminal outputs a third ANDed signal;

a sixth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the fifth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the sixth D-type flip-flop is enabled, and the byte output terminal outputs a sixth delay byte data;

a seventh D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the sixth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the seventh D-type flip-flop is enabled, and the byte output terminal outputs a seventh delay byte data;

a eighth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the seventh delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the eighth D-type flip-flop is enabled, and the byte output terminal outputs an eighth delay byte data;

a ninth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the eighth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives

the third ANDed signal so that the ninth D-type flip-flop is enabled, and the byte output terminal outputs a ninth delay byte data; and

a tenth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the ninth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the tenth D-type flip-flop is enabled, and the byte output terminal outputs a tenth delay byte data.

Regarding claim 20, the circuit of claim 1, wherein the write-in buffer controller further comprises:

an OR gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives one of the pointer signals, the second input terminal receives the non-idle data cell signal and the output terminal outputs an ORed signal;

a first AND gate having a first input terminal, a second input terminal, a third input terminal, a fourth input terminal and an output terminal, wherein the first input terminal receives the ORed signal, the second input terminal receives one of the state signals, the third input terminal receives another one of the pointer signals, the fourth input terminal receives the data stream enable signal and the output terminal outputs a first ANDed signal;

a second AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the first ANDed signal, the second input terminal receives a write-in request signal from the buffer and the output terminal outputs the write-in signal; and a third AND gate having an input terminal, an inversion input terminal and

an output terminal, wherein the input terminal receives the first ANDed signal, the inversion input terminal receives the write-in request signal and the output terminal outputs the overflow signal.

Regarding claim 22, the method of claim 21, wherein the method further includes a header data correction step for submitting a correction code to the descrambler when the header contains a bit error and the correction code is obtained from a correction table according to the syndrome code of the header.

Regarding claim 23, the method of claim 21, wherein the byte-wise data pipeline receives data according to the following steps:

a data cell reception step for receiving any data bytes within the data cell;

a header cyclic redundancy code elimination step for disabling a first portion of the byte-wise data pipeline holding principle header data and preventing any header cyclic redundancy code from passing into the byte-wise data pipeline; and

a header cell elimination step for disabling a second portion of the byte-wise data pipeline for a period after the passage of header cyclic redundancy code into the byte-wise data pipeline is blocked but the passage payload cell data into the byte-wise data pipeline is continued so that header cell data shifting into the remaining area of the byte-wise data pipeline is avoided.

Regarding claim 24, the method of claim 21, wherein the method further includes a first data cell counting step for counting the number of data cell received since the last state transition

according to the pointer signal provided by the byte pointer and assessing the need for a transition into the full synchronization state before the cell delineation state machine actually transits from the search state into the full synchronization state.

Regarding claim 25, the method of claim 21, wherein the method further includes a second data cell counting step for counting the number of data cell received since the last state transition according to the pointer signal provided by the byte pointer and assessing the need for a transition back to the search state before the cell delineation state machine actually transits from the full synchronization state into the search state.

Regarding claim 26, the method of claim 21, wherein the pointer signal outputting step further includes the utilization of a pointer signal from the byte pointer and a secondary state signal from the synchronization state machine for equalizing the pointer signal corresponding to the first byte data of the payload cell and the pointer signal corresponding to the header cyclic redundancy code.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-3141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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